A Fast Data-Acquisition System for a Time-Shared Computer

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Abstract—Computer-aided testing is usually performed with a dedicated computer, typically adding a five-digit number to the cost of the test equipment. In such systems the computer sets the test conditions and then records the test results from digital meters. This approach can lead to intolerably slow measurements when the dedicated computer is replaced by a remote time-shared computer. This paper discusses a solution to the problem in which an inexpensive interface (under 1000 dollars) sets the test conditions locally, so that a long string of data can be transmitted to the computer when the telephone line is open. A typical application is the evaluation of high-power microwave transistors, using a standard network analyzer. Connected to a Teletype, the system covers up to 40 frequency points in about 20 s, and displays the calculated and corrected *S*-parameters within another 20 s. If connected to the computer line through a 1200 Bd line, the system is speeded up by a factor of approximately 10.

INTRODUCTION

COMPUTER-AIDED testing (CAT) has not only become a way of life for many engineers, but a large segment of the electronics industry could no longer exist without it. Manufacturers of logical circuits chips must frequently perform hundreds of tests per dollar of product value, and an expensive CAT system is consequently justified. As engineers in other electronic fields have whetted their appetites by using the computer more and more as a design tool, they too begin to appreciate the speed, accuracy, and low cost of computer assistance, and are anxious to see this powerful tool applied to the experimental phase of their work. At present test data are usually displayed either on meters or oscilloscopes. If additional manipulation of these data is needed, they must be recorded and either fed into a computer by hand or subjected to hand calculation. Obviously, this process not only constitutes a waste of costly manpower, but also introduces errors and inaccuracies. Furthermore, and perhaps most significantly, the effort involved encourages the use of raw data rather than corrected or derived quantities.

These problems are particularly severe in the field of microwave engineering, because practically only power and voltage can be measured directly. All other parameters, such as impedance or phase, must be derived. Furthermore, microwave measurements are inherently inaccurate. Errors of 10 percent or more are the rule, and calibration procedures are an essential part of every microwave measurement. Incorporation of calibration data is, however, frequently cumbersome if not altogether impractical. For these reasons, the advent of computer-coupled test equipment (such as the Hewlett-Packard Network Analyzer) has been hailed as the beginning of a new era in microwave engineering.

Unfortunately, the cost of progress is, in this instance, unusually high. Computerization of test equipment usually adds between 10 000 and 100 000 dollars to its cost and frequently provides only very limited computational capabilities. Utilization of available time-sharing facilities thus becomes an economic necessity where either a substantial number of test stations can benefit from computerization, or when a time-shared computer is already available. Because these criteria fit a vast number of applications in many fields of engineering, one might logically expect data interfaces to be easily available. As a result of the wide range of specific requirements of the test equipment, as well as the computer systems, this development was, however, very slow and, when the Advanced Technology Laboratory of the RCA Electronic Components Division needed a data acquisition system, no suitable equipment could be found on the market. Although several firms now endeavor to fill the need for data couplers along the lines described above, we are still far from a simple "plug-in and run" situation. The required modifications and debugging efforts on commercially available components, and the high cost of the more versatile units, will in many cases still favor the homemade system.

Typically, data-acquisition systems use various digitally controlled devices such as power supplies, generators, or attenuators to establish the test conditions. The resulting output data are then inputted to the computer, and new test conditions are established. If the output data volume is small (e.g., one 3-digit value each for the real and imaginary component of a complex quantity), the above approach to CAT can become intolerably slow because of the low data rate of most terminals, the time needed to turn around telephone lines, and—last but not least—the queuing delays inherent to time-shared computers.

A data-acquisition system designed for this environment must therefore feed as much information to the remote computer as possible, when the computer is in the "receive" mode. Because most engineering tests use at least one independent variable (e.g., frequency) against which the dependent variable (e.g., impedance) is plotted, one solution is to increment the independent variable locally and feed the results of one full-frequency sweep to the computer at once. This approach has the added advantage that the test station does not become inoperable when the computer is unavailable, but can

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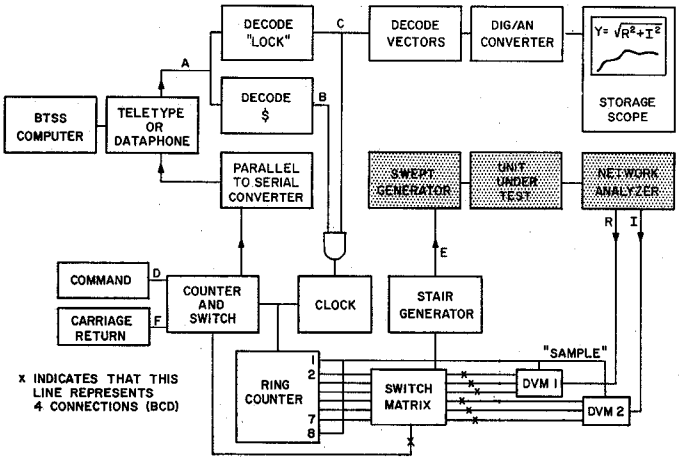

Fig. 1. Block diagram of the data acquisition system MATE. Shaded components are external to MATE.

still scan and display "raw" data. With the failure record of many present time-sharing systems this is more than just a fringe benefit. Being capable of manual as well as automatic operation, the equipment was dubbed "MATE" (manual/automatic test equipment). For convenience, this acronym will now be used in the present paper.

As the display unit, MATE uses the "Model T" developed by Miller and Wine at the RCA David Sarnoff Research Center [1]. The Model T utilizes a storage oscilloscope as the display device to plot graphs, or present other graphic outputs obtained from the RCA basic time-sharing system. With some minor modifications the Model T is also used to decode the command symbol which starts MATE, and to convert the output data from parallel to serial form. The interaction of the major components is described in the following section.

The Basic Circuit

Fig. 1 shows a block diagram of the MATE system; its operation will be described by an example. The test equipment is assumed to be a network analyzer, fed from a sweep generator, so that frequency is the independent variable. The outputs are the real and imaginary parts (*RR* and *RI*) of the reflection coefficient; the coefficient is available from the polar display unit of the network analyzer in the form of two voltages between −1 and +1 V. For demonstration purposes, the magnitude of the reflection coefficient (*RM*) will serve as the quantity to be displayed on the storage oscilloscope at 40 frequencies.

The computer program for this, written in Fortran PI [2], is shown in Fig. 2. During execution when the symbol $ (hexadecimal 44) is printed on the terminal (sequence no. 90), it also appears (in serial form) at point *A*. This symbol is decoded and generates a logical ONE at point *B*. The Model T is still locked, so that another ONE appears at point *C*, and the AND gate turns on the clock. The clock is connected to a ring counter (RC) in which a logical ONE (+5 V) is moved at every clock beat by one position. It may be assumed that this

```
 10    GLOBALREAL R(40),I(40),A,X,Y,BUF(87)
 20 1  FORMAT('S',N)
 30 2  FORMAT(I1,40(2F3.0))
 40    A=101; BEGINNING OF MODELT CALL
 50    CALL MODELT(A)
 60    A=4.
 70    X=0; INITIALIZATION FOR PLOT
 80    CALL MODELT(A)
 90 4  PRINT1
100    READ 2 KO,(R(J),I(J),J=1,10*KO)
110    DO5 J=1,10*KO
120    CALL CALC(J)
130    X=J/KO
140    A=12; DESIGNATES PLOTTING SYMBOL "SQUARE"
150 5  CALL MODELT(A)
160    GOTO 4
170    SUBROUTINE CALC(J)
180    Y=SQRT(R(J)/1000)**2+(I(J)/1000)**2)
190    RETURN
200    END
```

Fig. 2. A simple program to demonstrate the operation of MATE, written in PIFOR.

bit was loaded into position 6 (by means of a reset button) before execution was started. The first clock pulse now moves the bit into position 7 and simultaneously closes a switch which connects the command digit (selected on a Digiswitch) at point *D* to the parallel-to-serial (P/S) converter. This digit is now read by the computer under the READ statement (sequence no. 100) as *KO*.

The next clock pulse moves the 1 into the next position (labeled 8 and 1) where it causes the stair generator to feed the first test voltage, corresponding to frequency $F(1)$, into the sweep generator (point *E*). The unit under test (UUT) now generates the readings $R(1)$ and $I(1)$ at the outputs *R* and *I* of the network analyzer. Simultaneously the sample inputs of the two digital voltmeters are enabled, each of which has one binary-coded decimal (BCD) output for each of its three digits.

When the next clock pulse moves the 1-bit to position 2, the digital voltmeters (DVMs) hold their readings, and the first digit of the first voltmeter is connected to the P/S converter, and thereby to the computer. This procedure is now repeated for the remaining 5 digits, thus completing the first set $R(1)$ and $I(1)$ of the READ statement. The next clock pulse raises the voltage in the stair generator to the second level, corresponding to $F(2)$, and the 6 digits are scanned again. The whole cycle is repeated until the counter reaches a preset value, for example, 40. The counter now connects the P/S converter to point *F* which provides the carriage return (hexadecimal *ØD*). When the computer receives the *ØD*, it empties its buffer and continues execution of the program.

The DO loop, sequence nos. 110 to 150, calculates the values $Y(J)$ to be displayed on the scope by calling SUBROUTINE CALC. In the example, this quantity is simply the geometric sum of the *R* and *I* readings. When the array $Y(J)$ is available, the Model T subroutine is applied; this subroutine is contained in the memory of the RCA time-sharing system [1]. When the graph is completed, the whole cycle, starting with sequence no. 90 repeats itself, while the operator may make adjustments (for example, to minimize the reflection coefficient) on the UUT.

It should be noted that the number of frequency points covered by the READ statement is determined by

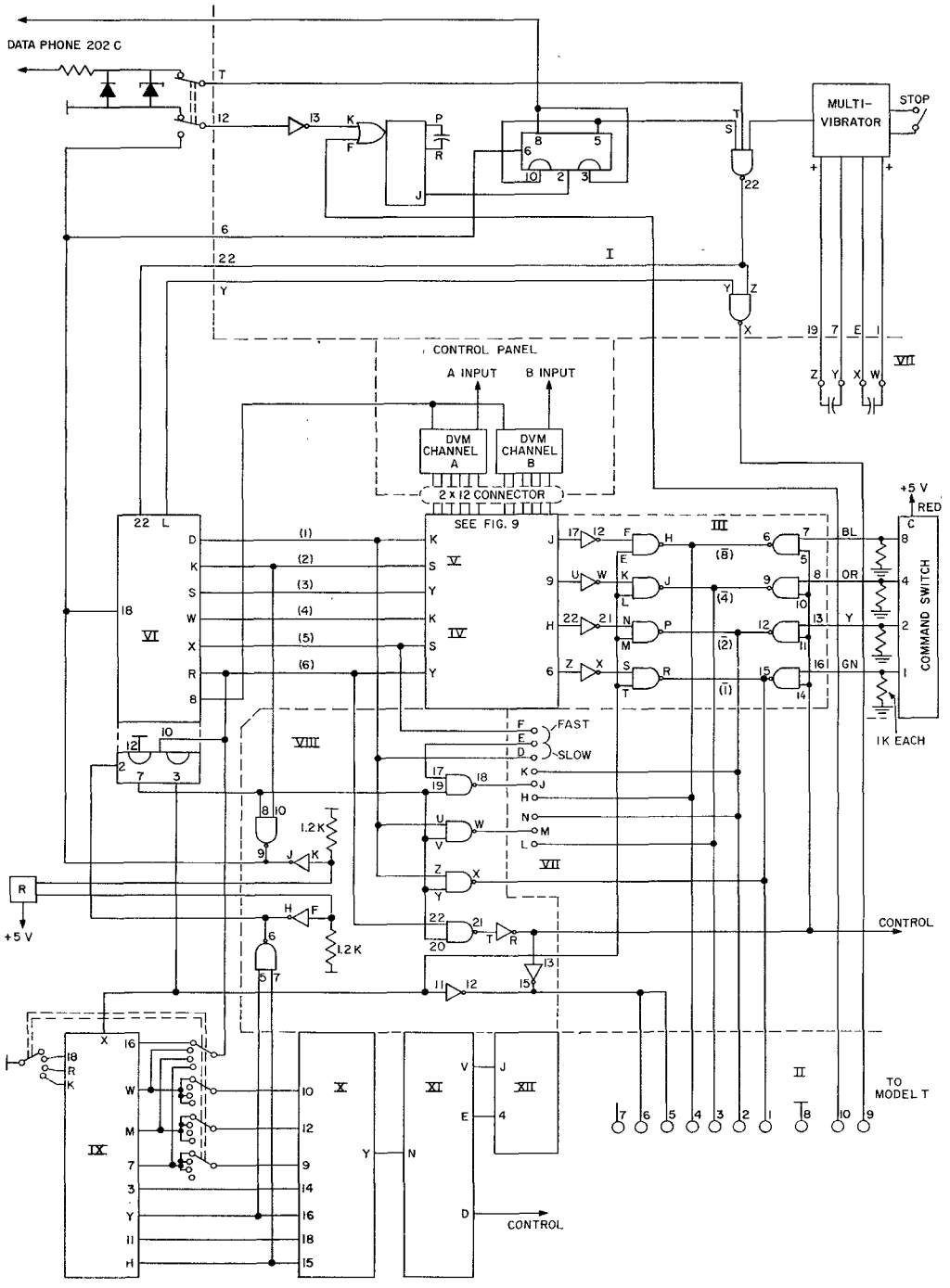

Fig. 3. Overall schematic of the logic circuits used in MATE, excluding the Model T circuitry.

the setting of the command switch. In this simple example the value of *KO* would be restricted to values from 1 to 4, because 40 frequency steps yield 240 output digits, and the capacity of the input buffer at the remote computer is 256 bytes.

If packed BCD numerals were used to transmit the measured data to the computer, as many as 64 frequencies could be accommodated. The data flow could then, however, contain byte sequences which are reserved as control characters for the input buffer of the remote computer. It was therefore decided to transmit the data in ASCII form which has the additional benefit of making the data printable on the local terminal. As MATE was designed for research and development work rather than routine testing, the immediate availability of the raw data is well worth the price of a somewhat reduced data rate.

Circuit Description

Datascan, Inc. circuit boards [3] were used in the construction of MATE; their function is described briefly below. The schematic diagram shown in Fig. 3 identifies

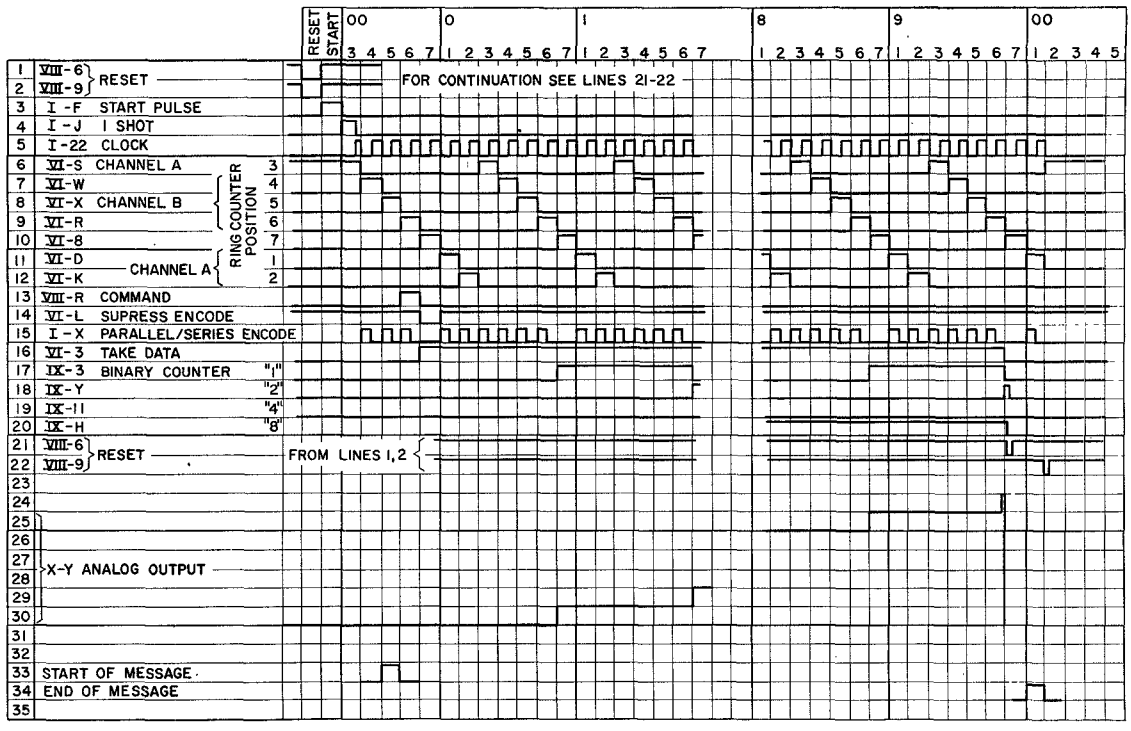

Fig. 4. Timing diagram of the MATE logic.

the boards by Roman numerals, while letters and arabic numerals identify connector pins. Decoding of the start signal ($) and P/S conversion of the output digits are performed within the Model T (not shown in Fig. 3).

The *Clockboard* (I) supplies the clock pulses for MATE. The multivibrator frequency is determined by the *Timer Board* (VII), so that either 10 or 120 characters per second can be scanned, depending on whether 110 or 1200-Bd transmission is used.

The *Ring-Counter Board* (VI) is a shift register. One of its flip-flops is used for control purposes.

The *Binary Counter* (1X) is used to count to 10, 20, or 40, depending on where the ring-counter pulses are applied. After reading the desired count, this board terminates the scan cycle.

The *Stair Generator* (X) converts the binary outputs of the counter (IX) to an analog signal, thereby generating the stair function which represents the independent variable. This signal is converted from the range of 0 to +5 V to a range of −10 to +10 V by the *Operational Amplifier* (XI), which also supplies sufficient power to drive a 5000-Ω load.

The heart of the data-acquisition system is the *Switching Matrix Boards* (IV and V) containing 12 NAND gates per board. Each of these boards accommodates the 3 BCD digits from one DVM. Other NAND gates boards connect the command switch to the system (III), and supply punctuation characters (VIII), i.e., carriage return (hexadecimal *ØD*) at the end of a 110-Bd transmission, or start message (hexadecimal Ø2) and end of message (hexadecimal Ø3) at beginning and end, respectively, of a 1200-Bd transmission. Except for the "handshaking" circuitry [4], which turns around the telephone connection, all connections with the telephone system go to the Model T. Incoming signals are directly acceptable to the Model T while outgoing signals must be converted. For the slow speed, this conversion is performed with a reed relay, while for the high-speed transmission (via Dataphone 202C), a simpler transistor circuit performs the conversion.

The functioning of the MATE circuit (Fig. 3) is best discussed in conjunction with the timing diagram in Fig. 4. The fast operating mode (1200 Bd) is assumed because it is somewhat more involved.

Before execution of the computer program is started, the system is readied by depressing the reset button *R*, which zeroes the binary counter and loads a 1 into the appropriate position (point VI-*S*) of the ring counter. The start signal ($) is applied to I-*F* which, after a 50-ms delay, causes the flip-flop output (I-5) to change to 1. This output is also connected to pin 4 of the Dataphone, model 202C. The positive voltage at this pin constitutes a request to send, which causes the carrier to be turned on in the Dataphone. When the Dataphone is clear to send, the voltage on its pin 5 turns from negative to positive. Thus point I-*T*, which so far was held to 0 by a diode, goes positive, and the clock pulses appear at I-22. The time delay is required to give the telephone equipment time to stabilize, and the handshaking process is completed.

When the clock starts, flip-flop output VI-3 is a binary 0 (ground) which indicates the 00 condition of MATE. This state occurs at the beginning and end of the scan cycle; it is used to apply punctuation characters. When

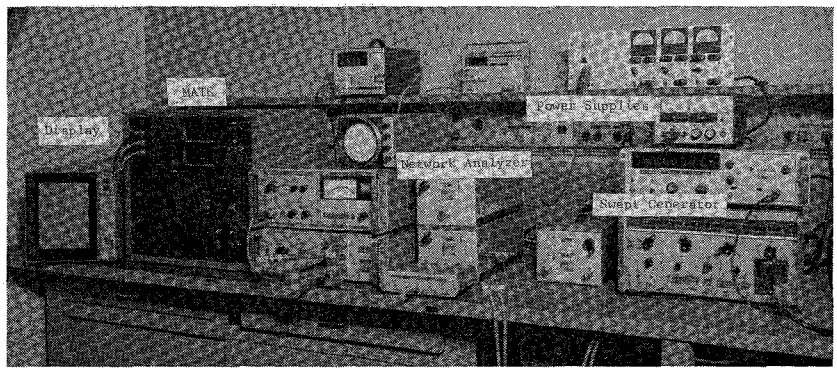

Fig. 5. MATE in its usual place.

step 00 coincides with ring-counter position 5, the NAND-gate output VIII-18 goes low, and the complement of hexadecimal Ø2 is applied to the P/S converter of the Model T. This character signifies start of message (line 33, Fig. 4) to the computer, which, in the 1200 Bd mode, disregards all signals arriving before the hexadecimal Ø2. The next clock pulse activates ring-counter output VI-*R*, which connects the command switch to the P/S converter because III-5, 10, 11, and 16 go high.

The next clock pulse switches the flip-flop output VI-3 to 1, and the first step in the scan cycle begins. The stair voltage has not changed so far, and, therefore, the current state can be identified as step 0. Ring-counter position 7 now causes the DVMs to sample, while positions 1 through 6 connect the DVM digits to the P/S converter, as indicated in lines 6 through 12 of Fig. 4. Because flip-flop output VI-3 (line 16) is now high, the binary counter is counting, and the next 1 to 0 transition from ring-counter position 6 raises the stair voltage to step 1. Sampling and scanning proceed as before, until the stair has reached step 9.

When at the end of step 9 the binary counter reaches 1010 · · ·, NAND-gate output VIII-6 goes to ground, and the flip-flop output VI-3 follows (line 16 in Fig. 4). Thus the 00 condition is again obtained. When it coincides with ring-counter position 1, the NAND-gate outputs VIII-*W* and -*X* apply the complement of hexadecimal Ø3 to the P/S converter. This signal indicates end of message, which is equivalent to the carriage return in the 110-Bd mode. The BTSS buffer is now emptied, while MATE resets itself, as evidenced by lines 22 and 6 in Fig. 4, thereby becoming ready to respond to the next start signal. Fig. 5 is an overall view of MATE in its usual place. To make MATE as universally applicable as possible, two identical inputs (channel *A* and channel *B*, top left) are provided with a variable offset voltage and variable voltage divider (knobs between input jacks and DVMs). This permits the inputs to be adjusted to the range from 0 to +1 V needed by the DVMs. A calibration switch permits quick checking of the offset voltage, which would normally be set to 0.5 V. Similarly, the step-voltage output is adjustable and provided with an offset voltage.

The control panel provides one important convenience: by means of a Local switch (top right), the connected test equipment can be operated independently of the computer. In this case, the horizontal scope deflection is taken directly from the step generator, and the vertical deflection from either channel *A* or channel *B*. At the end of the scan cycle the 1-shot pulse shown on line 4 in Fig. 4 is used to erase the scope and start a new scan cycle. The Local feature is not only insurance against computer failures, but permits leisurely calibration of the test set and occasional reversion to the raw data when the display of the calculated quantity looks suspicious.

Application of MATE

Although MATE was designed to automate a wide range of engineering tests, its use will be described below in its most important application to date; namely, the interfacing of a Hewlett-Packard network analyzer with the RCA time-sharing system. The major components of the test set are identified in Fig. 5, as it is used to measure the *S*-parameters of the RCA microwave transistor 7487 at different operating points. This transistor is used in an *S*-band power amplifier with a linear output of 0.5 W at 3 GHz [5].

In order to obtain hard-copy outputs, the measurements were performed in the slow (10 characters per second) mode. (The Teletype console itself is located behind the wall at the left in Fig. 5.) Figs. 6 and 7 are the printouts from one session, when the *S*-parameters were taken between 2.4 and 3.3 GHz, at collector currents of 175, 100, and 50 mA, respectively.

The sequence of events is recorded in Fig. 6 in the first digits following the $ sign, which correspond to the positions of the command switch of MATE. The assignments were:

0 null calibration;
1 calibration with matched load;
2 calibration with short;
3 calibration with offset short;
4 calibration with both ports shorted;
5 calibration with ports connected directly;
6 data for input-reflection coefficient S11;
7 data for reverse-transmission coefficient S12;

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$0503505503505503505503505503505503505503505503505503505503505
$0158505158505158505158505158505158505158505158505158505158505
$0500846500846500846500846500846500846500846500846500846500846
$5500849736771851553796312596174348210181387130636357809604831
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$9240760208722189683172637151591156555153509151469168436171389
$9237755206718187679170632150586155550153503152464170431173384
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K V1 V2

Fig. 6. Data transmitted to the RCA time-sharing system during one session. K indicates the command digit, $V1$ and $V2$ are the first readings from channel A and channel B, respectively.

F	RHO INP X 1.000*		REV.TRAN X 1.000*		TR.-COEF X 1.000*		RHO OUTP X 1.000*	
2.400	0.86	155.72	0.11	82.56	1.05	-161.67	1.05	-133.73
2.500	0.83	154.24	0.12	75.79	1.02	-169.30	1.04	-135.50
2.600	0.82	151.38	0.13	69.96	1.01	-179.80	1.02	-137.91
2.700	0.81	149.35	0.14	65.25	1.03	170.75	1.01	-140.50
2.800	0.79	146.45	0.15	59.54	0.97	161.46	0.99	-142.63
2.900	0.79	143.23	0.16	53.53	0.96	151.12	0.97	-144.89
3.000	0.78	140.25	0.16	48.31	0.90	141.84	0.96	-147.19
3.100	0.78	137.20	0.16	43.24	0.85	133.31	0.94	-149.55
3.200	0.77	134.33	0.17	37.75	0.78	126.39	0.93	-151.96
3.300	0.77	130.33	0.17	33.36	0.74	117.74	0.92	-154.50
2.400	0.87	154.89	0.12	82.72	1.30	-152.77	1.13	-133.32
2.500	0.85	152.34	0.13	77.14	1.29	-161.32	1.13	-135.68
2.600	0.84	149.30	0.14	70.51	1.27	-171.54	1.10	-138.43
2.700	0.83	147.06	0.15	65.81	1.29	178.76	1.08	-141.23
2.800	0.81	144.27	0.16	60.50	1.16	-23.71	1.06	-143.55
2.900	0.80	140.77	0.17	53.44	1.24	158.09	1.04	-146.13
3.000	0.79	137.91	0.17	47.64	1.14	148.49	1.02	-148.65
3.100	0.79	134.64	0.17	43.13	1.06	140.13	1.00	-150.97
3.200	0.78	131.62	0.18	38.77	1.00	132.69	0.98	-153.59
3.300	0.78	127.71	0.18	34.44	0.93	124.43	0.97	-156.13
2.400	0.86	156.09	0.12	85.28	1.21	-156.70	1.13	-132.89
2.500	0.84	153.77	0.12	77.30	1.20	-164.73	1.12	-134.94
2.600	0.83	151.02	0.13	71.32	1.20	-175.43	1.10	-137.43
2.700	0.82	149.10	0.15	66.33	1.19	175.56	1.08	-140.36
2.800	0.80	146.18	0.15	61.38	1.16	165.38	1.06	-142.72
2.900	0.79	143.33	0.17	54.58	1.16	154.96	1.04	-145.26
3.000	0.79	139.89	0.17	48.97	1.06	145.51	1.02	-147.64
3.100	0.78	137.60	0.17	43.93	0.98	137.04	1.00	-150.17
3.200	0.78	134.28	0.17	38.27	0.92	129.36	0.98	-152.71
3.300	0.78	130.42	0.18	34.44	0.87	121.31	0.97	-155.28

READY
1610

Fig. 7. Printout of the corrected S-parameters, obtained from the raw data recorded in Fig. 6.

8 data for forward-transmission coefficient S21;
9 data for output-reflection coefficient S22.

The calibration steps were repeated after the transmission coefficient data because of temporary operator disconnect. In Fig. 7 the resulting S-parameters are printed out by magnitude and angle using the RCA network-analysis program ASPIC. This program is employed to calculate the S-parameters at the actual chip connection so that the data can be taken through a matching network rather than in a 50-Ω system. It is also possible to display and print the gain which an amplifier of a given configuration would have if this specific transistor was used in it. This requires substantial computational capability; a dedicated minicomputer could not handle it in addition to the calibration program and the plotting routine.

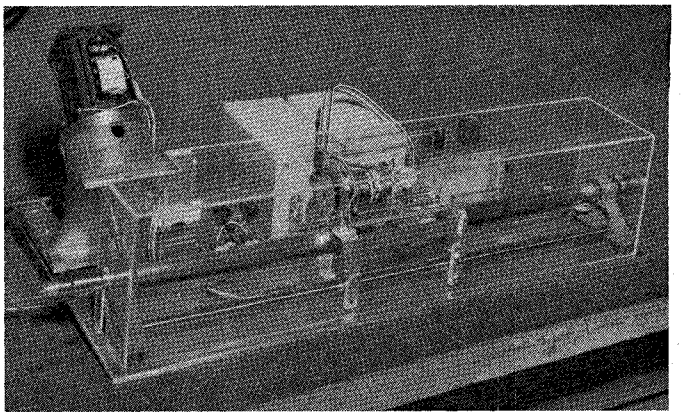

Fig. 8. Computer-activated double-slug tuner used in the compilation of load-sensitivity data.

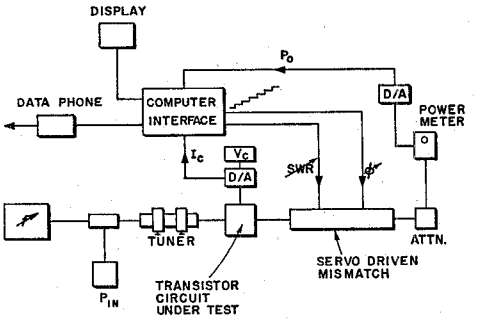

Fig. 9. Schematic of the load-sensitivity test equipment, using MATE and a semiautomatic double-slug tuner.

While S-parameters are today the generally accepted characteristics of microwave transistors in the linear region, class C application poses quite different problems. At the RCA Advanced Technology Laboratory a special double-slug tuner has been constructed, which will permit the use of MATE for the semiautomatic compilation of load-pull diagrams. These diagrams consist of power output contours superimposed on a Smith chart. They indicate at a glance with what complex load a given transistor wants to operate, and how this operating point should change with frequency. The compilation of load-pull charts over a range of frequencies, drive levels, dc voltages, and input impedances presents a task that could not possibly be tackled without computer assistance. Fig. 8 is a photograph of the computer-controlled double-slug tuner, and Fig. 9 shows the schematic. A typical load-pull diagram is depicted in Fig. 10. Some of the work that has been done with the help of MATE is described in the literature [5]–[7].

Conclusions

A data acquisition system (MATE), which feeds engineering test data into a time-shared computer, has been constructed from inexpensive logic cards. This equip-

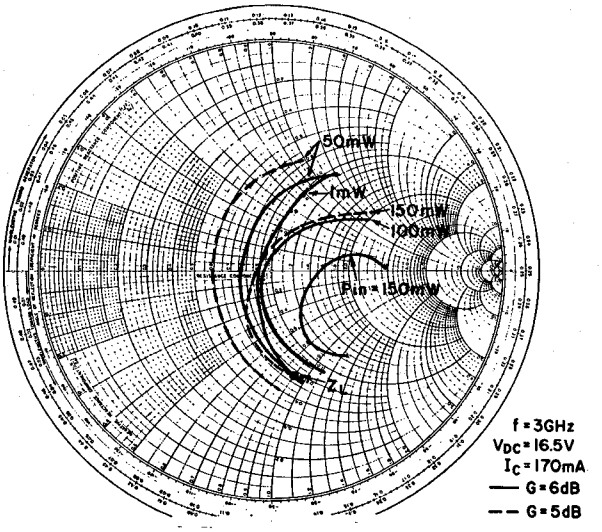

Fig. 10. A typical load-sensitivity diagram.

ment generates, upon computer command, a stair voltage representing the independent variable. Two DVMs read 3 digits each of the independent variables at every step of the stair function so that up to 240 digits of test data can be fed into the computer within seconds.

The equipment has so far been applied primarily to interface a Hewlett-Packard network analyzer with the RCA time-sharing system. The stair voltage is used to step up the frequency (from a sweep generator), which thus becomes the independent variable, or to activate an automated double-slug tuner. The dependent variables are two voltages representing the real and imaginary part of the quantity which the network analyzer monitors at the time. By setting a command switch to the appropriate value, the operator informs the computer which quantity is being read, and the corrected quantity is immediately displayed on a storage oscilloscope. When the measurement is completed, a local terminal produces hard-copy output.

Because of the self-sweeping feature of MATE, this equipment can perform tests at the same speed as a dedicated computer provides, but with the computational capability of a large computer and the small operating cost of a time-sharing system. This approach to computer-aided testing thus represents a very attractive alternative to the use of a small dedicated computer. The simplicity of MATE furthermore provides a substantial economic advantage over more versatile commercial systems.

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